SPEED NEGIOTIATION DEVICE AND METHOD

ABSTRACT OF THE DISCLOSURE

A device and method for data rate selection in data transmission is provided, having a first register for storing an N bit data upon clocking by a first clock; a second at least one register for storing the N bit data upon clocking by a second clock, the second clock having a clock rate of two times the clock rate of the first clock; a circuit for receiving the N bit data output from the first register and outputting a first half of the N bit data during a first phase of the first clock and outputting a second half of the N bit data during a second phase of the first clock; and a multiplexer for receiving as first inputs the output of the circuit and second inputs the output of the second at least one register, wherein the multiplexer outputs the first inputs as a lower speed data and outputs the second inputs as a higher speed data based on a rate select signal.